MOS (PTY) LTD.

Microsystems On Silicon

Member of ELMOS Semiconductor AG

E910.62
Dual Channel
PIR Signal Processor

General Description

The E910.62 integrated circuit is designed for interfacing Passive Infra Red (PIR) sensors with micro-controllers or processors. A single wire **D**ata **O**ut, **C**lock **I**n (DOCI) interface is provided for interfacing with a micro-controller. Multiple devices can easily be operated at the same time.

Up to two PIR sensors elements connect directly to the PIR inputs. The PIR signal is converted to a 14 bit digital value.

The E910.62 contains an on chip temperature measurement circuit with a resolution of better than 0.1K. The PIR sensor voltages and the temperature value are supplied to an external microcontroller through the DOCI interface.

Applications

- Integration with PIR sensor elements (hybrid modules)
- Gas sensors
- High end PIR systems

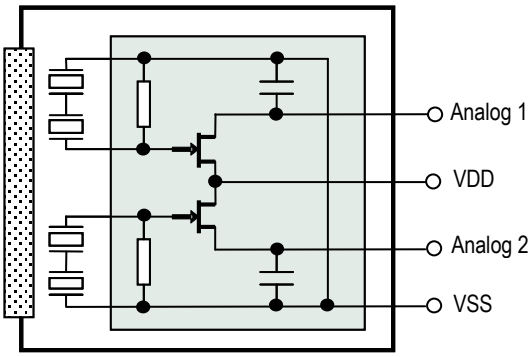
Features

- Direct connection to PIR sensor elements
- Temperature measurement
- Differential PIR inputs
- Digital Signal Processing (DSP)
- Single wire serial interface (DOCI™)
- Operating voltage down to 2.7V
- Low current consumption
- High dynamic range
- High supply rejection

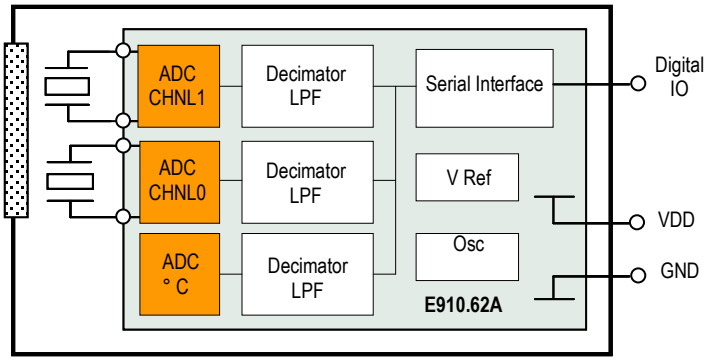
Digital Sensor Assembly with E910.62

The E910.62 PIR Signal processor replaces the JFETs and optional discrete components. The pin count of the detector is reduced to 3 pins.

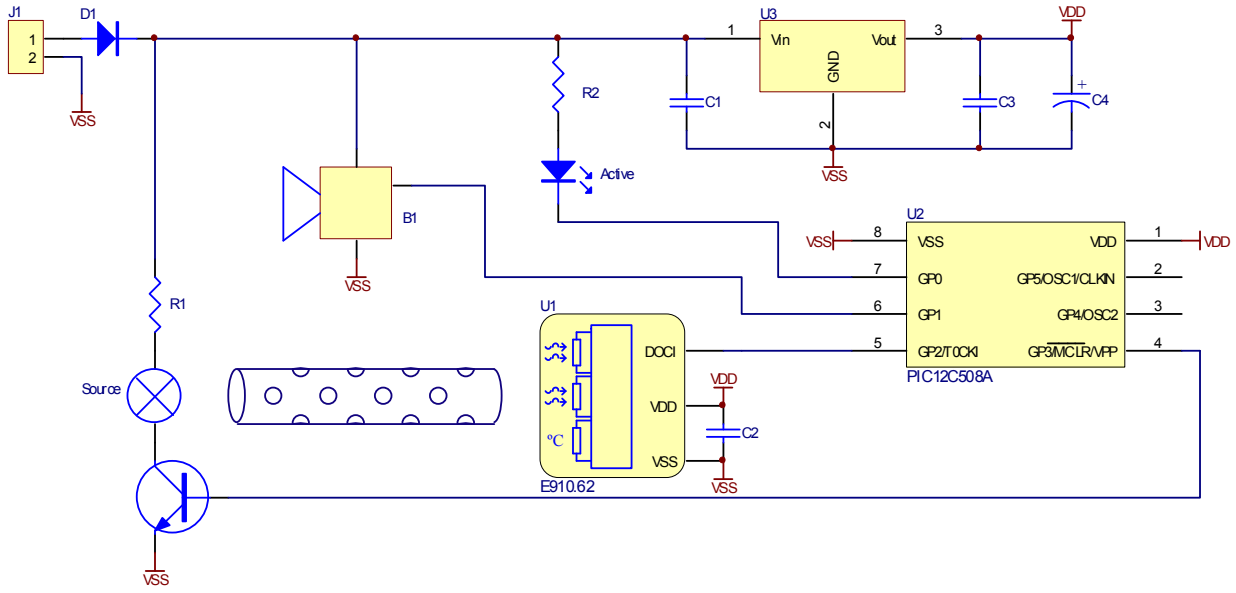
Traditional analog PIR detector



New digital PIR detector



Application Diagram for a Gas Sensor



Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remarks
Supply Voltage	V_{DD}	-0.3	3.6	V	
Current into any pin		-100	100	mA	One pin at a time
Storage Temperature	T_{st}	-45	125	°C	

Stresses beyond those listed above may cause permanent damage to the device. Exposure to absolute maximum ratings may affect the device reliability.
ESD protection: all pins will be able to withstand a discharge of a 100pF capacitor charged to 1.6kV through a 1500Ω series resistor. Test method: MIL-STD-883D method 3015.

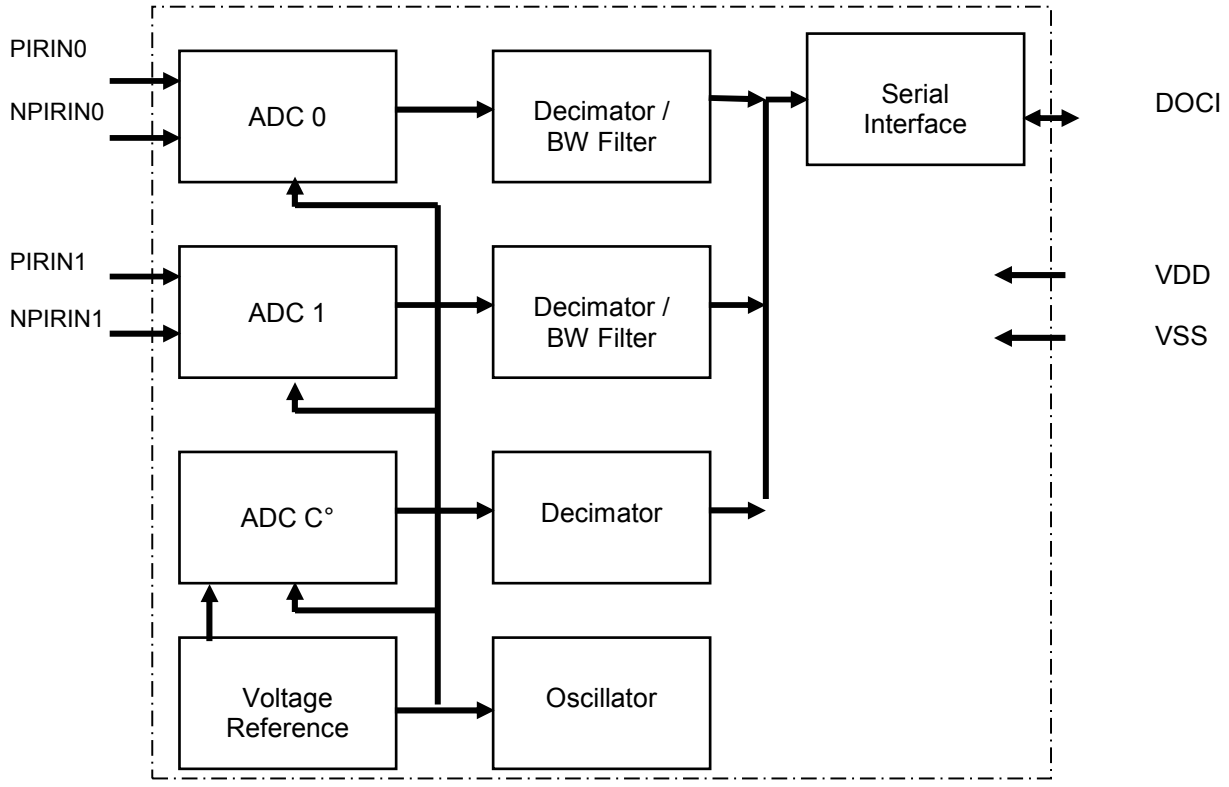
Operating Conditions (T=25°C, V_{DD}=3Vunless stated otherwise)

Operating temperature range: -25 to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Supply						
Supply voltage	V_{DD}	2.7	3.3	3.6	V	
Supply current	I_{DD}		13.5	18	µA	V_{DD}=3.3V
Digital DOCI interface						
Input low voltage	V_{IL}			20	%V_{DD}	
Input high voltage	V_{IH}	80			%V_{DD}	
Pull down current			200		µA	IN/Out to V_{DD}
Pull up current			130		µA	IN/Out to V_{SS}
Input capacitance			5		pF	
Data setup time	t_s	2			$1/F_{CLK}$	
Data clock low time	t_L	200			ns	
Data clock high time	t_H	200			ns	
Data bit settling time	t_{bit}	1			µs	C_{LOAD} = 10pF
Serial Interface update time	T_{REP}		512		$1/F_{CLK}$	
Analog Inputs PIR+, PIR-, Analog to Digital Converter						
Input leakage		-1		1	fA	V_{IN} = -10mV .. +10mV
PIRIN input voltage range		-50		50	mV	Differential
		-100		100	mV	Common Mode
ADC Resolution			14		Bits	Max Count = 2^14-1
ADC Sensitivity		6	6.5	7.1	µV/count	
ADC Temperature Coefficient		-300		300	ppm/K	
RMS output noise referred to input			2.5		µV	@ 0.5Hz
			1.5		µV	@ 1Hz
			0.5		µV	@ 2Hz
			0.4		µV	@ 5Hz
ADC Offset		7000	8192	9200	counts	
Digital Filter Type & Cut off Freq.	F_0	F_{CLK} * 1.41 / 2048 / PI			Hz	2nd Order BW LPF
Digital Filter Sampling Freq.	F_S		1/32		F_{CLK}	
DOCI Interrupt cycle	T_I		512		$1/F_{CLK}$	

Temperature Measurement						
Measurement Range		-20		+90	°C	
Resolution		72	80	88	Counts/K	
Linearity		-5		5	%	-20°C to +90°C
Count Value at Ambient		5700	6700	7700	Counts	@ 25°C
Oscillator						
Internal Oscillator Frequency	F_{OSC}		70		kHz	
Internal clock frequency	F_{CLK}		$F_{CLK}/2$			
Temperature Dependency		-500		500	ppm/k	-20°C to +80°C

Detailed Description



Oscillator

The IC contains an on chip low power oscillator, with a frequency of 70 kHz. All time related signals and the cutoff frequencies of the digital filters are related to the oscillator's frequency.

PIR Inputs and A/D Conversion

The analog to digital converter generates a digital signal from the voltage level measured between the PIRIN and NPIRIN terminals.

The output signal from the ADC is converted to a 14 bit value by down sampling to Fclk/32.

Temperature Measurement

The on chip temperature is measured by converting the temperature dependent voltage of the reference to a digital value with a resolution of better than 0.05K.

Parallel to Serial Data Latch

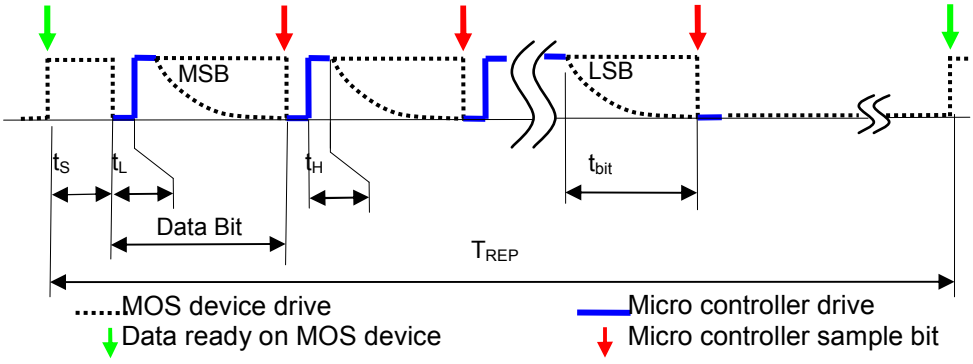
New data is transferred from the decimators to the serial interface every 32 system clocks, if the DOCI output is at low level and not active (being read). If the micro controller reads the register faster than the update rate of the filter, the data read is "0".

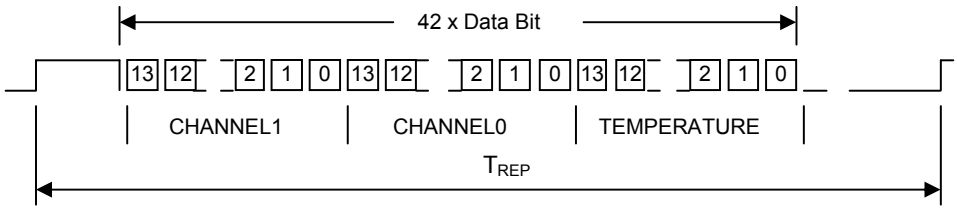
The E910.62 generates an interrupt every 512 system clock cycles, if the microcontroller reads all 42 bits within 32 system clock cycles. The interrupt is indicated by the E910.62 by pulling DOCI high.

The microcontroller must wait for 1us. It then generates a low to high transition on the DOCI line, before it samples the data bit. The first bit read is the MSB. This process is repeated until all 42 bits have been read. After the last bit is read, the microcontroller must force low level and subsequently release DOCI.
If reading is interrupted for more than 32 system clocks with the DOCI interface at low level, the output data latch is updated with new values. Reading can be interrupted, while the DOCI interface is forced high. The output latch is not updated in this condition.

The E910.62 accepts readout with µC defined timing. The interrupt signal can be ignored and reading frequency can be up to FCLK/64. In this mode, the µC has to force DOCI to a high level for the duration of 3 device clock cycles (3/FCLK) and subsequently read out the data bits as described in the timing diagram below.
The readout can be terminated at any time by forcing the DOCI interface to low level and release it thereafter.

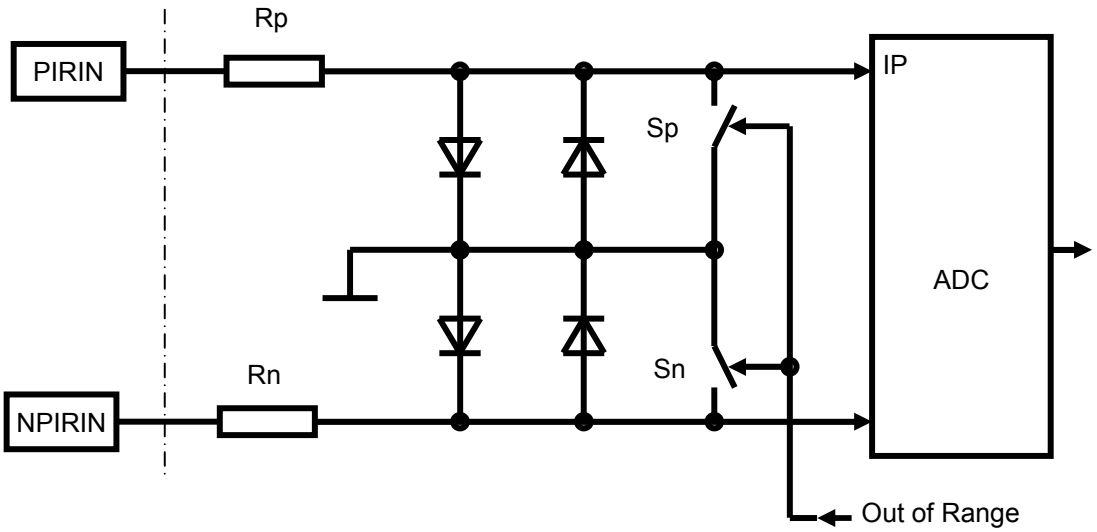
DOCI Interface





T_{REP} = 512 system clocks

ADC Input Stage

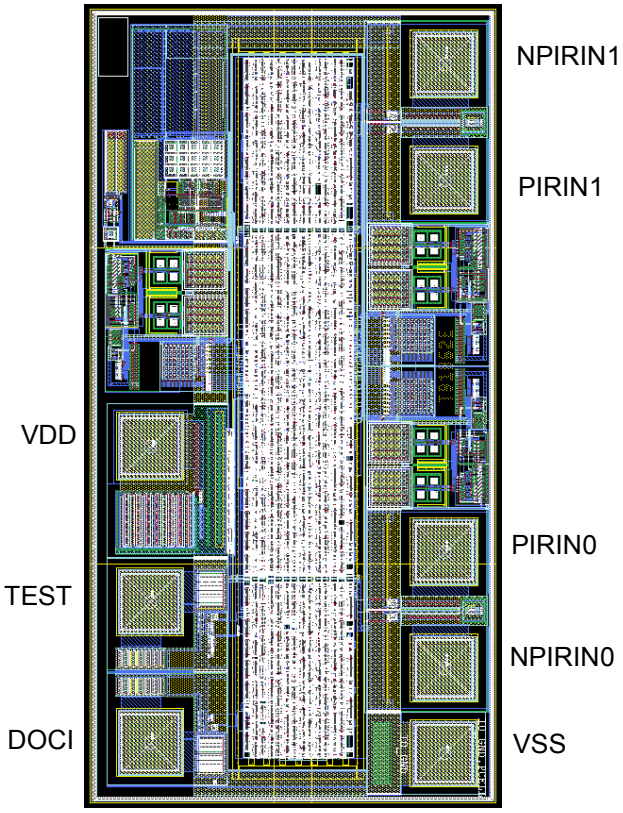


Out of Range Detection

The dynamic range of the ADC Input stage is approximately +/- 50mV. To avoid saturation, the E910.62 contains out of range detection logic, which detects values above 15872 (97% of range) and below 511 (3% of range). If the values are outside this range, the switches Sp and Sn are closed for the duration of 512 system clocks. This ensures fast settling after disturbances.

The input impedance of the actual ADC (IP / IN) is practically infinite.

Pad Positions



Pad	X	Y
DOCI	0	23
TEST	0	260
VDD	0	520
VSS	530	0
NPIRIN0	530	145
PIRIN0	530	340
PIRIN1	530	960
NPIRIN1	530	1150
Chip Dimensions	710	1330

Values are in µm

Contact Information

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