E910.97
Integrated Circuit for PIR Smart Sensor

General Description

The E910.97 integrated circuit combines all required functions for a single chip Passive Infra-Red (PIR) motion detector.
Motion detection is signaled through the push-pull REL output. A digital input OEN enables REL output.
The E910.97 interfaces directly to a PIR sensor element via a high impedance differential input. The PIR signal is converted to a 15 bit digital value.
The parameters for sensitivity and timing are set by connecting the corresponding inputs to DC voltages. The voltage levels on the inputs are converted to digital values with 7 bit resolution.
All signal processing is performed digitally. The E910.97 bare die is for assembly with a pyro-ceramic element in a hermetically sealed package.

Applications

PIR motion detection
Intruder detection
Occupancy detection
Motion sensor lights

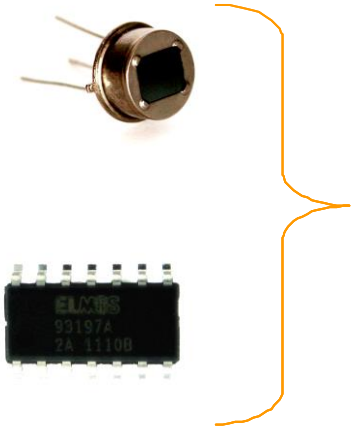
Features

Digital signal processing
On chip supply shunt regulator
Low power consumption
Differential PIR sensor input
Excellent power supply rejection
Insensitive to RF interference
Inputs for sensitivity and on time

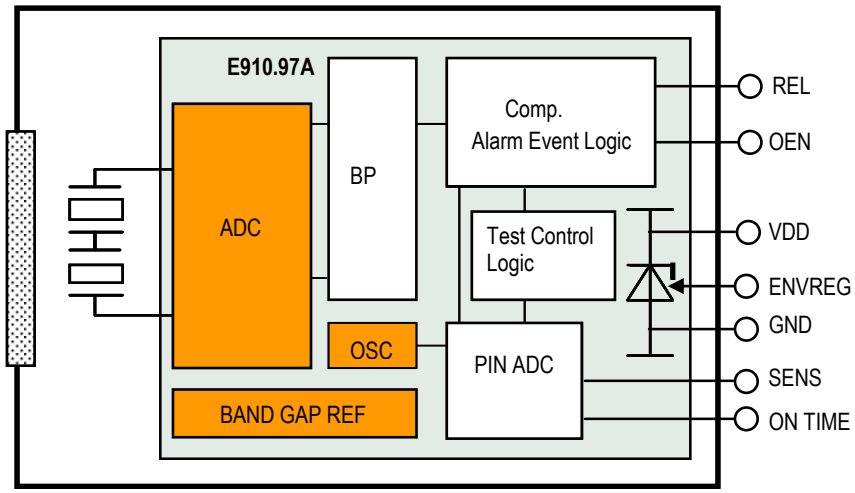
Smart Digital Sensor Assembly with E910.97

The E910.97 PIR Controller results in a single component Solution for a Motion Sensor

Traditional analog PIR Sensor solution



New Smart PIR Detector with E910.97



Six pin PIR Detector using E910.97

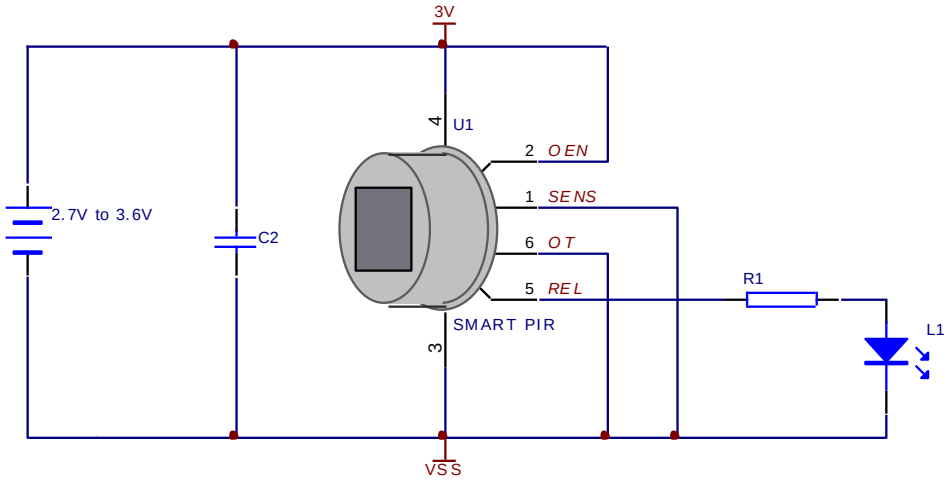


Fig.1: Minimum component final product PIR motion detector with LED indication

Comp	Typ. Value	Function	Note
U1		Smart Motion Sensor	Internal voltage regulator not used
R1	680R	Current setting resistor	
C2	470nF	Vdd-Vss Supply bypass capacitor	
L1		LED	

Table 1: Component values for minimum component solution

Mains Powered Motion Sensor Light Application Circuit

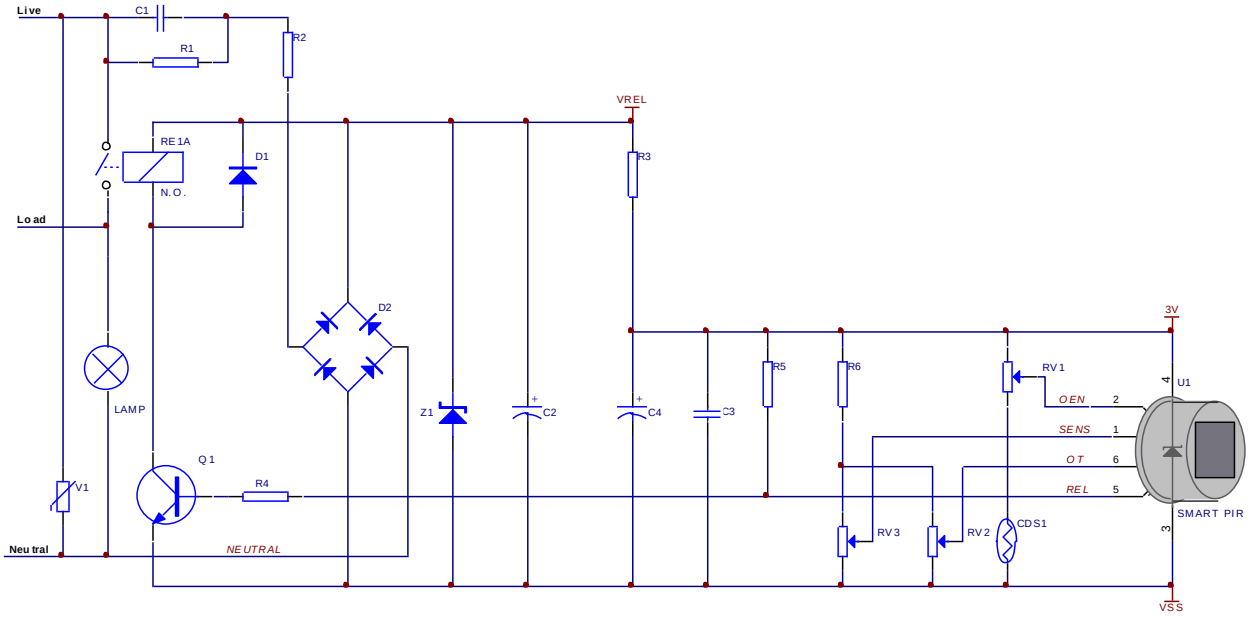


Fig.2: Schematic for mains powered motion sensor light

Designator	Typ. Value	Description	Note
U1		Smart Motion Sensor	Smart Sensor with E910.97, Internal voltage regulator enabled.
R1	1M	Discharge resistor	
R2	100R	Transient protection resistor	Wire wound
R3	56k	Current limiting resistor	R3 < $(V_{Rel}-V_{VDD})/(I_{IDD}+I_{R5}+I_{R6}+I_{VR1}+I_{R4})/1.5$
R4	12k	Transistor drive resistor	R4 < $(V_{Rel}-0.6)/(I_{REL}/\beta_{Q1})$
R5	47k	Current balance resistor	R5 < $V_{Rel}/(I_{REL}/\beta_{Q1})$ Equalizes current between REL=0 and REL=1
R6	270k	Voltage divider	R6 > 3 X 1/(1/RV2+1/RV3) x1.1
D1	1N4148	Fly back protection diode	
D2	DB104S	Diode bridge	
Z1	ZD47	47V Zener diode	Choose according to RE1 voltage,500mW
Q1	BC489B	Low cost NPN transistor	
CdS1		Light dependent resistor	
RV1	2.2M	OEN Voltage Adjust	
RV2	220k	Sensitivity adjustment	Select in conjunction with R6 and RV3
RV3	220k	On Time adjustment	Select in conjunction with R6 and RV2
V1	S10275VAC	Transorb, for high voltage spike protection	
C1	270n/230VAC	Voltage dropper capacitor	
C2	10µF	Supply voltage storage	Voltage rating dependent on RE1 voltage
C3	1µF	Decoupling capacitor	Ceramic, close to supply pins of device
C4	10µF	Sensor supply storage	Regulator compensation capacitor
RE1	47V	N.O. REL	High coil voltage, less drive current
S1		3 position Mains switch	

Table 2: Component Values for Motion Sensor Light

Electrical Characteristics

Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Exposure to absolute maximum ratings may affect the device reliability.

Parameter	Symbol	Min	Max	Unit	Remarks
Supply Voltage	V_{DD}	-0.3	3.6	V	
Current into any pin		-100	100	mA	One pin at a time
Storage Temperature	T_{st}	-45	125	°C	

Table 3: Maximum Ratings

ESD protection: all pins except PIRIN and NPIRIN will be able to withstand a discharge of a 100pF capacitor charged to 1.6kV through a 1500Ω series resistor. Test method: MIL-STD-883D method 3015.

Operating Conditions

The parameters listed below for normal operation and are specified for an ambient temperature of 25 degree Celsius.

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Temperature						
Operating temperature range		-25		85	°C	
Regulator (Test conditions)*						
Shunt regulator current	I_R			5	mA	
Supply current, ENREG=VDD	I_{DD}			40	µA	VDD < Regulator voltage, Outputs unloaded
Supply current, ENREG=VSS	I_{DD}			15	µA	Regulator not active, VDD = 3.3V (Bond option)
Regulator voltage	V_{DD}	2.7		3.3	V	I_R = 0.5mA (Test condition)
Output REL						
Output current high	I_{OH}	-10			mA	$V_{OL}>(V_{DD}-1V)$
Output current low	I_{OL}	10			mA	$V_{OL}<1V$
Output active (On) time	t_{REL}	2		4194	s	16 steps
Input OEN						
Input low voltage	V_{IL}			0.6	V	
Input high voltage	V_{IH}	1.2			V	
Digital test-mode	V_{IDT}	V_{SS}-0.6		V_{SS}-0.4	V	
Analog test-mode	V_{IAT}	V_{DD}+0.4		V_{DD}+0.6	V	
Input Current	I_I	-1		1	µA	$V_{IN} = V_{SS} .. V_{DD}$
Input Current – Analog test mode	I_{AT}			20	µA	V_{IAT}=-0.5V
Input Current – Digital test mode	I_{DT}	-20			µA	$V_{IDT}=V_{DD}$+0.5V
Inputs SENS, ONTIME						
Input voltage range		0		V_{DD}		Adjustment between 0V and ¼ VDD
Input leakage current		-1		1	µA	
PIRIN / NPIRIN Inputs						
Input leakage		-1		1	fA	V_{IN} = -10mV .. 10mV
PIRIN input voltage range		-50		50	mV	Differential
		-100		100	mV	Common Mode
ADC Resolution			16		Bits	
ADC Sensitivity		1.6	1.8	2	µV/count	

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
ADC Temperature Coefficient		-300		300	ppm/K	
ADC Range		2048	32768	63488	counts	
ADC Offset		29500	32768	35700	counts	
ADC Noise	V_{NP}			5	Counts	Peak value
PIRIN /NPIRIN input resistance differential		100			GΩ	V_{IN} = -60mV .. 60mV
Oscillator and Filter						
LPF cutoff frequency	F_L	F_{CLK} * 1.41 / 2048 / PI			Hz	2nd Order BW
HPF cutoff frequency	F_H	F_{CLK} * 1.41 / 32768 / PI			Hz	2nd Order BW
Digital LPF Sampling Freq.	F_S		1/32		F_{CLK}	
On chip oscillator frequency	F_{OSC}	50	56	62	kHz	@25°C
System Clock	F_{CLK}		F_{CLK}/2			
Threshold Detector						
Threshold for pulse count	V_{THR}	104		516	µV	128 steps @ 3.25µV/step, hardwired offset of 32 steps = 104uV
DOCI Timing in test mode readout						
DOCI interrupt available	t_S	200			ns	Time MCU takes before register is read
Data clock low time	t_L	200			ns	
Data clock high time	t_H	200			ns	
Data bit settling time	t_{bit}	1			µs	C_{LOAD} = 10pF
Next word cycle	T_{REP}		32		1/ F_{CLK}	
Self-test Initialize	T_{ST}	8			1/ F_{CLK}	

Table 4: Operating Conditions

Test circuits shown for Device IDD and regulator measurements. Applications that make use of the internal regulator need to choose a current that satisfies constraints set by thermal performance of the detectors.

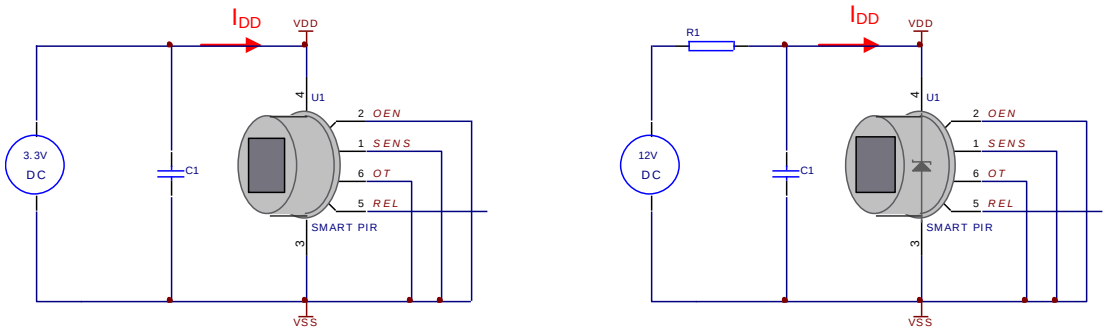


Fig.3: I_{DD} test circuits

Detailed Description

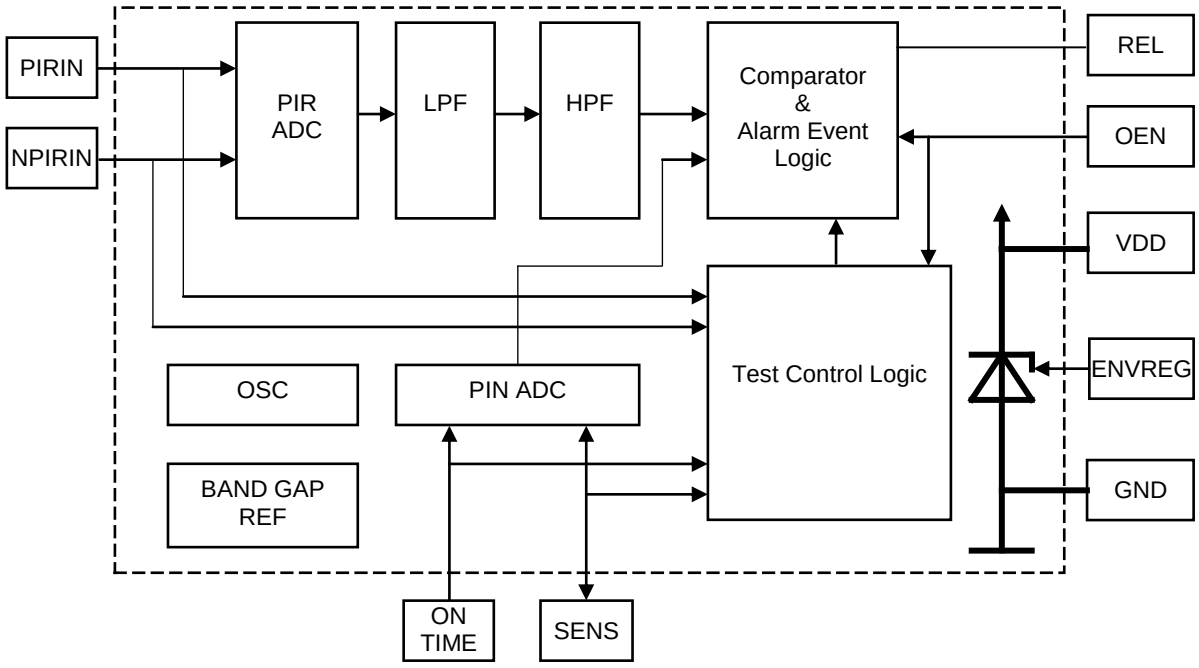


Fig 4: Block diagram of E910.97

PIR Sensor Input

A differential input stage provides for a direct connection to a high impedance PIR sensor element. The analog to digital converter generates a digital signal from the voltage level measured between the PIRIN and NPIRIN pins.
A band gap reference ensures a temperature and supply voltage independent gain.

Voltage Regulator

The on-chip shunt regulator accepts a large range of input currents. It generates a stable 3V supply for the internal circuitry. The V_{DD} pin requires a bypass capacitor to V_{SS}. The reference for the shunt regulator is taken from the integrated band gap reference.

Oscillator

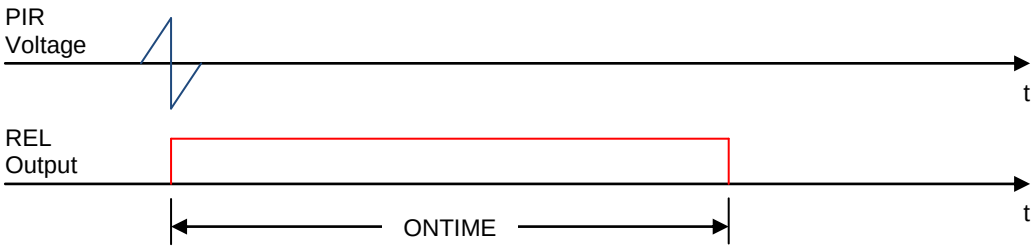
The IC contains an on chip low power oscillator. The frequency is set to 56kHz. The timing signals and cutoff frequencies of the digital filters are derived from this frequency. The oscillator clock frequency is divided by 2 for the internal system clock F_{CLK}.

Band-Pass Filter

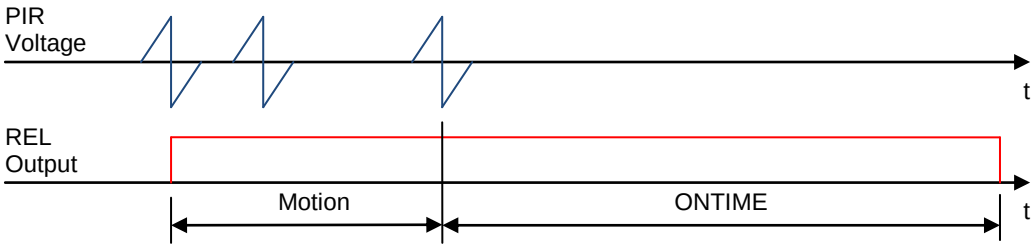
A 2nd order low-pass filter (LPF) with a cut-off frequency of 7Hz eliminates unwanted higher frequency components. This signal is then passed to a 2nd order high pass filter (HPF) with a 0.4Hz cut-off frequency.

Alarm Event Processor

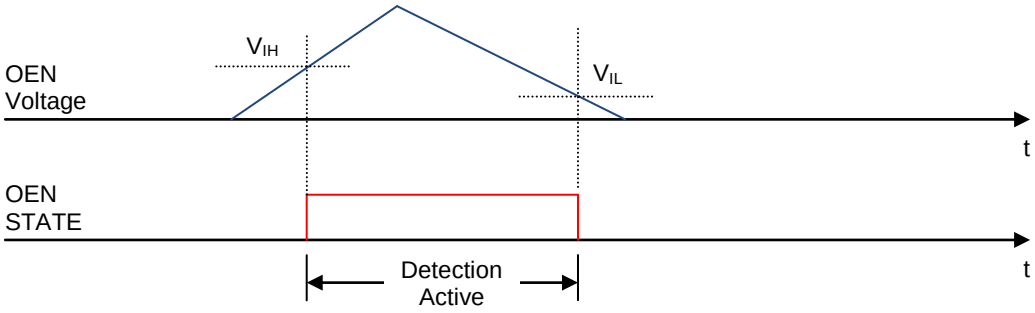
The signal from the band pass filter is rectified. When the signal level exceeds the set sensitivity threshold, an internal pulse is generated. A second pulse is counted, when the signals changes sign and exceeds the threshold again. Whenever 2 pulses appear within 4s, an alarm condition is detected and the REL output is activated. If the signal level is in excess of 5 times the selected threshold, 1 pulse will cause activation of the REL output.



REL output active due to single event



REL output active timing due to multiple events



Hysteresis on the OEN input

Fig 5: Timing diagram for motion

On Time

The voltage applied to the ONTIME input determines how long the REL output stays active after the last alarm condition has been detected. If multiple alarm conditions are detected during the on time period, the on time is re-started whenever an alarm condition is detected. The on time period is derived from the oscillator frequency and will have a spread accordingly.

Pin voltage Center of step voltage value	ON Time $F_{OSC\ Nom}$	ON Time $F_{OSC\ Max}$	ON Time $F_{OSC\ Nom}$	ON Time $F_{OSC\ Min}$
V_{DD}*3/128 or less	2	00:00:02	00:00:02	00:00:02
V_{DD}*5/128	5	00:00:04	00:00:04	00:00:05
V_{DD}*7/128	7	00:00:06	00:00:07	00:00:07
V_{DD}*9/128	9	00:00:08	00:00:09	00:00:10
V_{DD}*11/128	19	00:00:16	00:00:18	00:00:20
V_{DD}*13/128	37	00:00:33	00:00:37	00:00:41
V_{DD}*15/128	56	00:00:50	00:00:56	00:01:02
V_{DD}*17/128	75	00:01:07	00:01:14	00:01:23
V_{DD}*19/128	150	00:02:15	00:02:29	00:02:47
V_{DD}*21/128	300	00:04:30	00:04:59	00:05:35
V_{DD}*23/128	449	00:06:45	00:07:29	00:08:23
V_{DD}*25/128	599	00:09:01	00:09:59	00:11:11
V_{DD}*27/128	1198	00:18:02	00:19:58	00:22:22
V_{DD}*29/128	2397	00:36:04	00:39:56	00:44:44
V_{DD}*31/128	3595	00:54:07	00:59:55	01:07:06
V_{DD}*33/128 or above	4793	01:12:09	01:19:53	01:29:28

Table 5: DC input voltages and on time values

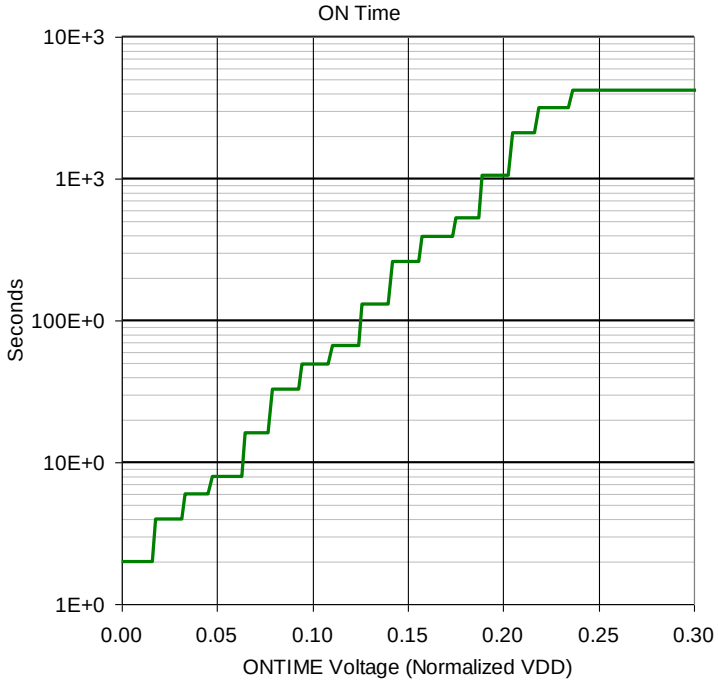


Fig. 6: REL Output on Time in seconds vs. ONTIME pin voltages normalized to VDD.

Sensitivity / Threshold

The voltage applied to the SENS input defines the threshold for the PIR signal which generates a pulse for the pulse counter, to determine an alarm condition. Connecting this input to VSS will result in the minimum possible threshold level, which is hardwired internally (offset) to avoid false detection due to zero threshold and detector noise. Any voltage above VDD/4 will select the maximum threshold, which is the least sensitive setting for PIR signal detection.

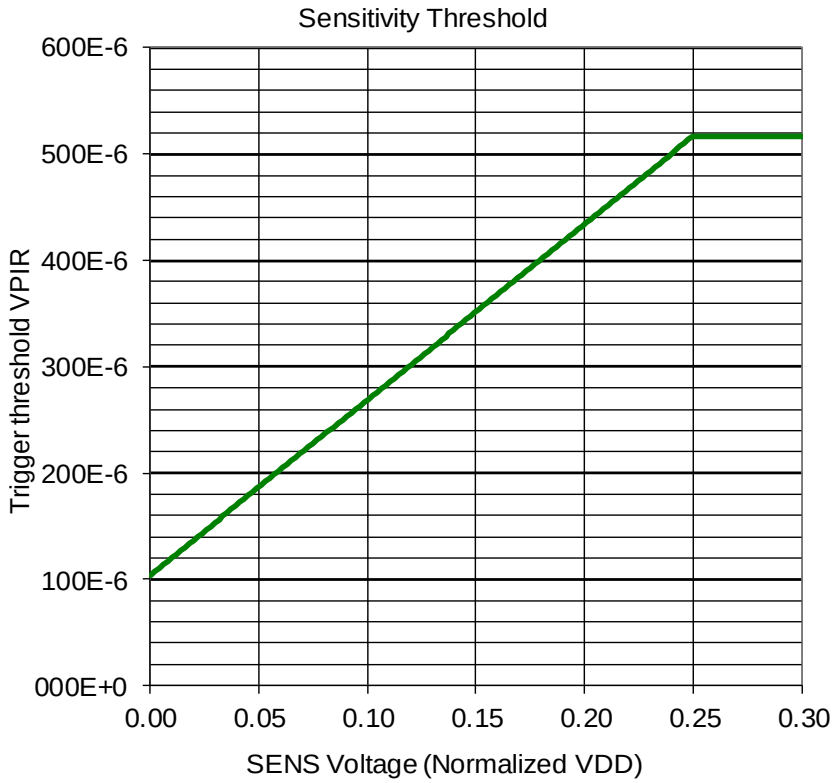


Fig. 7: PIR voltage trigger threshold vs. SENS pin voltages normalized to VDD.

Test Modes

There are 2 types of test modes implemented on the E910.97.

1. Chip Manufacturers Test Modes

These test modes are for chip test at the semiconductor manufacturer. They are not intended to be used anywhere else and are not described in detail.

2. Detector Manufacturers Test Modes

These test modes are implemented to aid the test of the assembled detector. They are aimed to shorten the test times and to detect faults in the connectivity between the integrated circuits and the externally connected pyro ceramic and Package pins. When performing a noise test by reading the ADC output on the device, once should consider the additional noise being generated due to crosstalk from the digital data to the pyro ceramic inside the detector housing. This test mode may also be used for the sensor manufacturer to verify the connections from the smart digital detector to his PCB.
However, it is not intended to use this test mode as normal operating mode in the final product.

INPUTS						**OUTPUT**	**MODE**
OEN	**ENVREG**	**SENS**	**ONTIME**	**PIRIN**	**NPIRIN**	**REL**	
Normal Operating Mode							
V_{SS} .. V_{DD}	ENVREG	SENS	ONTIME	PIRIN	NPIRIN	REL	Normal Operation
Chip Manufacturers Test Modes							
>V_{DD} +0.4v	ACLK	SENS	ONTIME	PIRIN	NPIRIN	DOCI, fast	Data Out – Clock in ATEST2
<V_{SS} -0.4v	TCLK	SENS	ONTIME	SDI	SCAN_EN	SCAN OUT	Digital Test DTEST
Detector Manufacturers Test Modes							
V_{SS} .. V_{DD}	ENVREG	SENS	>V_{DD} +0.4v	PIRIN	NPIRIN	DOCI	Parameter Test ATEST1
V_{SS} .. V_{DD}	ENVREG	SENS	<V_{SS} -0.4v	PIRIN	NPIRIN	DOCI	Initialize self test mode ATEST0

Table 6: Device test modes

DOCI Interface for ATEST1 and ATEST0

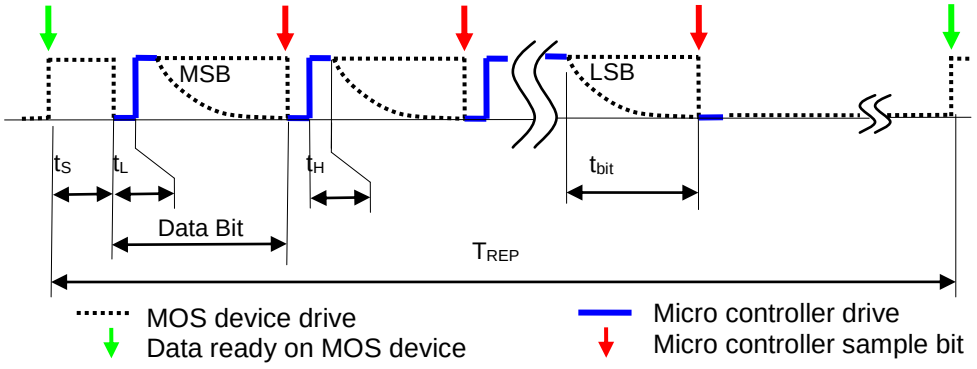


Fig 8: Timing diagram for the DOCI interface

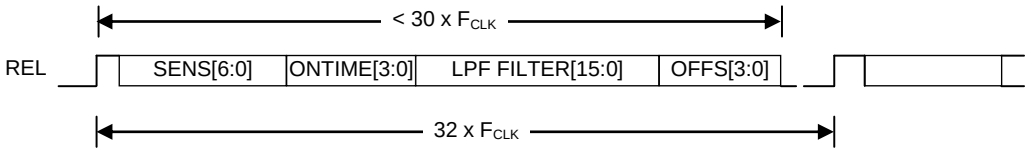


Fig. 9: DOCI data format for ATEST1 and self test (ATEST0)

Parameter Test ATEST1

In ATEST1 'Data Out – Clock in' (DOCI - LPF) - mode, the filter data and additional parameters are available as a 31 bit word on the REL output. Whenever a new filter value is generated, the REL output is switched to high level. Reading of data has to be completed in less than 30 system cycles after the REL output goes to VDD. The DOCI protocol is used to read the word. Reading of the data can be aborted at any time. A new read access can only be started after a new interrupt generated from the device (REL 0 to high).

LPF[15:0] contains the PIR Signal, after is has been digitized and processed by the digital low pass filter. The signal can be analyzed for offset and noise of the complete system and the sensitivity of the detector ceramic.

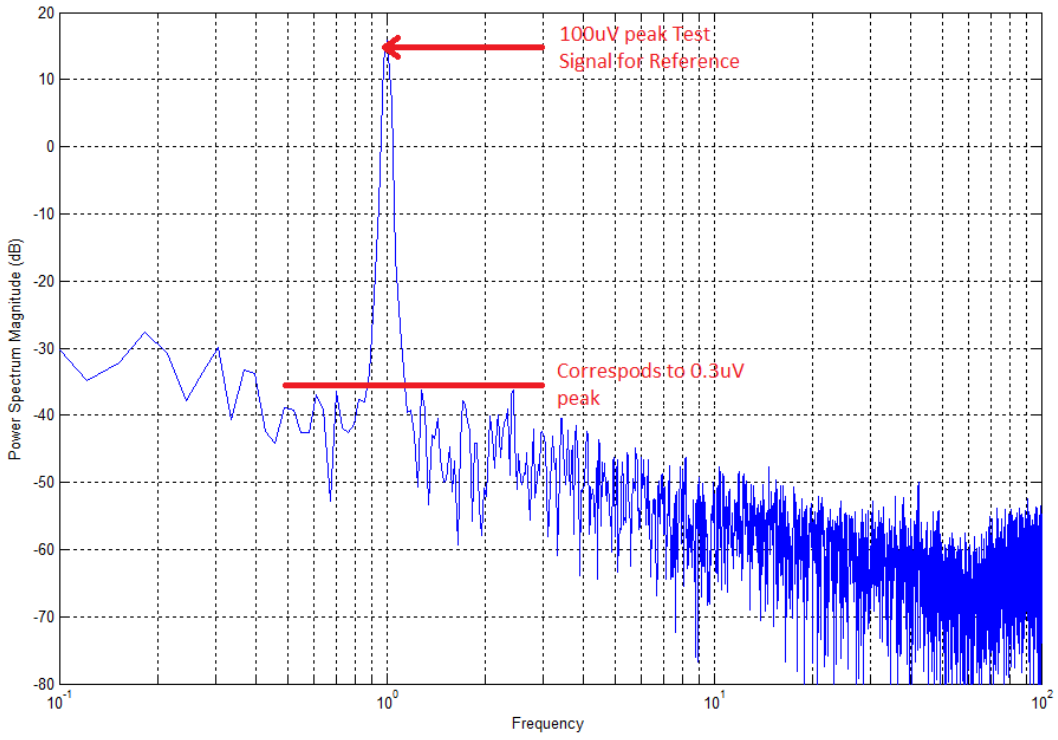


Fig. 10: Typical Noise Spectrum of ADC

Self-Test Initialize ATEST0

The self-test mode is initialized by applying a voltage of less than V_{SS}-0.4V to ONTIME, for at least T_{ST} and switching the device back to normal mode. (ONTIME = V_{SS} … V_{DD}) The device is now in self-test mode and the data format is as described for ATEST1. The following 2000 interrupts on the REL output will output the self-test voltages.
Captured readings must be evaluated against known good data limits, which were determined by the detector manufacture according to the capacitance and properties of the size and PYRO ceramic connected.
It is advisable to use only every 15th REL interrupt to minimize noise and amount of data to process.

Upon entering self-test mode the PIR inputs are alternatively connected to a switched capacitor circuit and charged up in steps. The PIR voltage is sampled and filtered on chip. After 2000 filter cycles the PIR inputs is put back in a normal detection state and self-test mode is exited automatically.

By plotting the FILTER[15:0] data on a graph a stair-step function will be shown, depending on the properties of the PYRO ceramic connected.

SENS[6:0] and ONTIME[3:0] contain the digital values for the corresponding pin voltages (SENS, ONTIME).
OFFS[3:0] are the upper bits of the hard wired offset for the threshold detector.

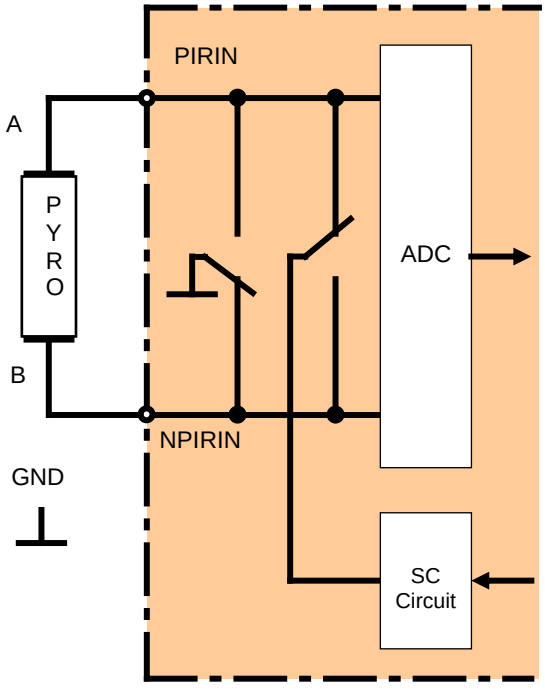
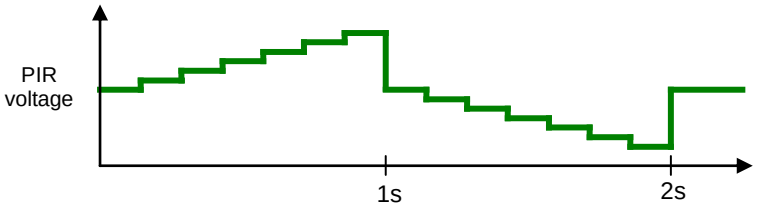


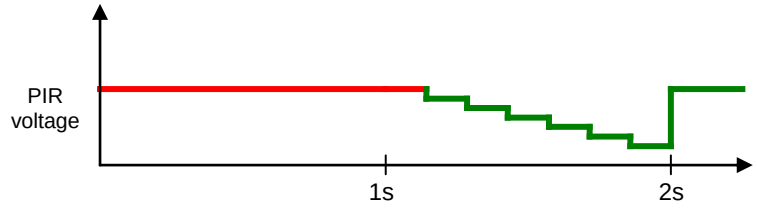
Fig. 11: Circuit for Self-Test

Self-test Results

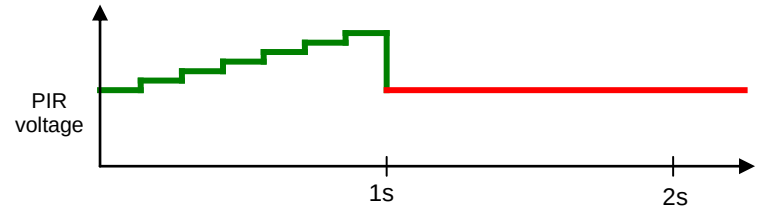
The data bits LPF[15:0] are used to analyze the conditions around the detector ceramic and the PIR inputs of the integrated circuit. The illustrations below explain the possible faults, which can be detected. The waveform may vary as a result of the characteristics of the detector ceramic. A bigger capacitance of the ceramic will result in smaller steps. A smaller capacitance may result in bigger steps and the voltage exceeding the dynamic range of the ADC.



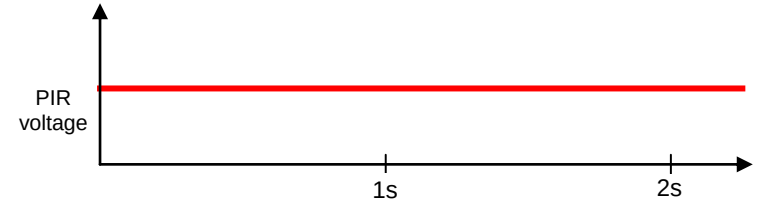
Good Detector



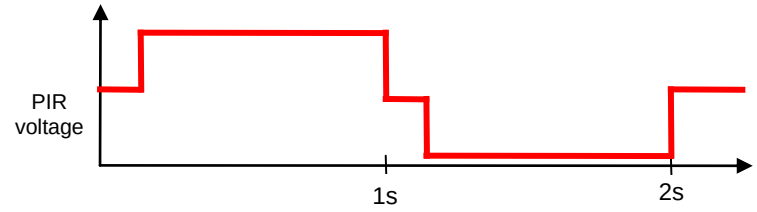
Short A/PIRIN to GND



Short B/NPIRIN to GND



Short A-B
or A and B to GND



PIRIN and NPIRIN
are unconnected
or ceramic broken

Suggested Pin out for Smart Digital Detectors

Pad Name	Type	DIP-14 Pin	T05-6 Pin	T05-4 Pin	Description
OEN	In	11	2	-	>1.2V: REL output is enabled <0.6V: REL output is disabled >(VDD+0.4V) or <(VSS-0.4V): Chip manufacturers test modes
V_{DD}	Supply	13	4	3	Supply voltage, internally connected to shunt regulator (active Zener)
NPIRIN	In	2	-	-	Negative PIR sensor input
PIRIN	In	1	-	-	PIR sensor input
V_{SS}	Supply	3	-	1	Negative supply voltage
ENREG	In	4	-	-	Shunt regulator enable, (Internal bond option, Bond to VDD to enable the regulator, Bond to VSS to disable the regulator for battery based applications.)
V_{DD}	Supply	5	4	3	Supply voltage
REL	Out	6	5	4	REL / motion detect output (push-pull)
V_{SS}	Supply	7	3	1	Negative supply voltage
SENS	In	10	6	-	Sensitivity selection input
ONTIME	In	9	1	2	On time selection input >(VDD+0.4V): ATEST1 Analog test mode <(VSS-0.4V): Initialize self test (ATEST0)

Table 7: Device Pin Out

Contact Information

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