# MOS (PTY) LTD.

Microsystems On Silicon

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## General Description\_

The E931.06 integrated circuit is designed for interfacing Passive Infra Red (PIR) sensors with micro-controllers or processors. A single wire Data Out, Clock In (DOCI) interface is provided for interfacing with a micro-controller. Multiple devices can easily be operated at the same time.

One PIR sensors ceramic elements connect directly to the PIR inputs. The PIR signal is converted to a 14 bit digital value.

The E931.06 contains an on chip temperature measurement circuit with a resolution of better than 0.05K. The PIR sensor voltages and the temperature value are supplied to an external microcontroller through the DOCI interface.

## E931.06 Single Channel PIR Signal Processor

## Applications

- Integration with PIR sensor elements (hybrid modules)
- High end PIR systems
- Building Management

## Features

- Direct connection to PIR sensor elements
- Temperature measurement
- Differential PIR Input
- Digital Signal Processing (DSP)
- ◆ Single wire serial interface (DOCI<sup>™</sup>)
- Operating voltage down to 2.7V
- Low current consumption
- High dynamic range
- High supply rejection

## Digital Sensor Assembly with E931.06\_

The E931.06 PIR Signal processor replaces the JFET and optional discrete components.

Traditional analog PIR detector



New digital PIR detector





## E931.06 Single Channel PIR Signal Processor





Fig 1: Typical application circuit for alarm motion sensor



## **Electrical Characteristics**

#### **Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Unit	Remarks
Supply Voltage	V <sub>DD</sub>	-0.3	3.6	V	
Current into any pin		-100	100	mA	One pin at a time
Storage Temperature	T <sub>st</sub>	-45	125	°C	

Stresses beyond those listed above may cause permanent damage to the device. Exposure to absolute maximum ratings may affect the device reliability.

ESD protection: all pins will be able to withstand a discharge of a 100pF capacitor charged to 1.6kV through a 1500Ω series resistor. Test method: MIL-STD-883D method 3015.

## **Operating Conditions (T=25°C, unless stated otherwise)**

Parameter	Symbol	Min	Тур	Мах	Unit	Remarks
		1	l	I	I	I
Supply	V	27	2.2	2.6	V	
Supply current	V <sub>DD</sub>	2.1	3.3	3.0 15	ν	\/3 3\/
	IDD		10	15	μΛ	VDD-0.0V
Digital DOCI interface						
Input low voltage	V <sub>IL</sub>			20	$%V_{DD}$	
Input high voltage	V <sub>IH</sub>	80			$%V_{DD}$	
Pull down current			200		μA	IN/Out to V <sub>DD</sub>
Pull up current			130		μA	IN/Out to V <sub>SS</sub>
Input capacitance			5		pF	
DOCI interface setup time	ts	2			1/F <sub>CLK</sub>	µC defines T <sub>REP</sub>
Data clock low time	tL	0.1		**	μs	** avoid update
DOCI low time	$t_L + t_{bit}$			1	1/F <sub>CLK</sub>	to avoid update
Data clock high time	t <sub>H</sub>	0.1			μs	
Data bit settling time	t <sub>bit</sub>	1			μs	$C_{LOAD} = 10 pF$
DOCI low time to ensure update	t <sub>vv</sub>	64			1/F <sub>CLK</sub>	
Analog Inputs PIR+, PIR-, Analo	og to Digita	al Conve	erter			
Input leakage		-1		1	fA	V <sub>IN</sub> = -10mV 10mV
PIRIN input voltage range		-50		50	mV	Differential
		-100		100	mV	Common Mode
ADC Resolution			14		Bits	512 2^14-512
ADC Sensitivity		6	6.5	7	µV/coun	
					t	
ADC Temperature Coefficient		-300	~ -	300	ppm/K	
RMS output noise referred to			2.5		μν	@ 0.5Hz
input			1.5		μV	@ 1Hz
			0.5		μν	@ 2Hz
		7000	0.4	0200	μV	@ 5Hz
		7000	8192	9200		
Digital Filter Type & Cut off Freq.		F <sub>CLK</sub> ^	1.41/20	148 / PI	HZ	2 Order BVV LPF
Digital Filter Sampling Freq.	⊢ <sub>S</sub>		1/32			
DOCI Interrupt cycle	T		512		1/ F <sub>CLK</sub>	





## E931.06 Single Channel PIR Signal Processor

**Temperature Measurement** 

Gain		70	80	90	Counts/K	-20°C to +90°C
Measurement Range		-20		+90	٥C	
Linearity		-5		5	%	-20°C to +90°C
Count Value at Ambient		5700	6700	7700	Counts	@ 25⁰C
Oscillator						
Internal Oscillator Frequency	Fosc	58	64	70	kHz	
Internal clock frequency	F <sub>CLK</sub>		F <sub>CLK</sub> /2			
Temperature Dependency		-1000		1000	ppm/k	-20°C to +80°C

Table 2: Operation conditions

## Detailed Description\_



Fig 2: Block diagram of E931.06

#### Oscillator

The IC contains an on chip low power oscillator, with a frequency of 64 kHz. All time related signals and the cutoff frequencies of the digital filters are related to the oscillator's frequency.

#### **PIR inputs and A/D conversion**

The analog to digital converter generates a digital signal from the voltage level measured between the PIRIN and NPIRIN terminals.

#### **Temperature Measurement**

The on chip temperature is measured by converting the temperature dependent voltage of

the reference to a digital value with a resolution of better than 0.1K.

#### **Decimation – Digital Filters**

The output signal from the PIR ADC is processed through a second order Butterworth low pass filter with a sampling rate of 1kHz.

The output signal from the Temperature ADC is converted to a 14 bit value by down sampling to Fclk/512.



#### Parallel to Serial Data Latch

New data is transferred from the decimators to the serial interface every 32 system clocks, if the DOCI output is not active (being read). If the micro controller reads the register faster than the update rate of the filter, the data read is "0".

#### Read on Device Interrupt

The E931.06A generates an interrupt every 512 system clock cycles ( $T_{REP}$ ), if the microcontroller reads all 28 bits within 32 system clock cycles. The interrupt is indicated by the E931.06A by pulling DOCI high.

The microcontroller must wait for 100ns (t<sub>s</sub>). It then generates a low to high transition on the DOCI line, before it samples the data bit. The first bit read is the MSB. This process is repeated until all 28 bits have been read. After the last bit is read, the microcontroller must force low level and subsequently release DOCI.

## E931.06 Single Channel PIR Signal Processor

If reading is interrupted for more than 1 system clock with the DOCI interface at low level, the output data latch is updated with new values. Reading can be interrupted, while the DOCI interface is forced high. The output latch is not updated in this condition.

#### Forced Read with uC Timing

The E931.06A accepts readout with  $\mu$ C defined timing. The interrupt signal can be ignored and reading frequency can be up to FCLK/64. In this mode, the  $\mu$ C has to force DOCI to a high level for the duration of >2 device clock cycles (>2/FCLK, t<sub>S</sub>) and subsequently read out the data bits as described previously and in the timing diagram below.

For the register to be updated, the  $\mu$ C must leave or force DOCI to low level for more than 64 system clocks (t<sub>W</sub>).

## DOCI Interface\_



Fig 3: Timing diagram for the DOCI interface



Fig 4: Data words available on DOCI interface

#### Summary for Operating the DOCI Interface

DOCI must be at "0" for >2ms to ensure a register update with new data. If DOCI remains "0" for more than  $512/F_{CLK}$ , the device will drive a weak "1" (max  $300\mu$ A).

The readout must start with a "1" for a duration of >100ns (interrupt) or 100us (force read).

The readout signal must be clean - any 010 or 101 glitches wider than 20ns may be treated as a data clock.

The low time of DOCI during readout must not exceed  $1/F_{CLK}$  to avoid updates during readout. Readout of data can be aborted at any time



## ADC Input Stage



Fig 5: Input structure of the ADC

#### Out of Range Detection

The dynamic range of the ADC Input stage is approximately +/- 50mV. To avoid saturation, the E931.06 contains out of range detection logic, which detects values above 15872 (97% of range) and below 511 (3% of range). If the values are outside this range, the switches Sp and Sn are closed for the duration of 512 system clocks. This ensures fast settling after disturbances.

The input impedance of the actual ADC (IP / IN) is practically infinite.



## Pad Names\_

Pad Name	Pin No.	TO5-3	Description
VSS	External	3	Negative supply voltage
NPIRIN	Internal	Int.	Negative PIR sensor input
PIRIN	Internal	Int.	Positive PIR sensor input
VDD	External	1	Positive Supply voltage
TCLK	Internal	Int.	Test clock, Leave Open
DOCI	External	2	Data Out Clock In, Soft driver, MCU interface
TEST	Internal	Int.	Test mode select, Leave Open

Table 3: Device Pin Out

## Pad Positions\_



Pad Name	X	Y
VDD	0.087	0.983
PIRIN	0.087	0.452
NPIRIN	0.087	0.257
VSS	0.087	0.084
TEST	0.524	1.049
DOCI	0.524	0.918
TCLK	0.524	0.687
Database	0.61	1.180

Table 4: Pad positions in mm

Fig 6: Die with pad names top view

## Contact Information

Microsystems On Silicon (Pty) Ltd. Pretoria, South Africa Tel: +27 12 998 4147 Fax: +27 12 998 4217 email: sales@mos.co.za Visit our website for the latest information