E931.08A
Single Channel Thermopile Signal Processor

General Description

The M931.08B integrated circuit is designed for interfacing Thermopile sensors with micro-controllers or processors. A single wire Data Out, Clock In (DOCI) interface is provided for interfacing with a micro-controller. Multiple devices can easily be operated at the same time.

One thermopile sensor connects directly to the analog inputs of the IC. The sensor signal is converted to a 17 bit digital value.

The M931.08B contains an on chip temperature measurement circuit with a resolution of better than 0.02K.

A 14 bit temperature value as well as a 17 bit sensor value is supplied to an external microcontroller through the DOCI interface.

Applications

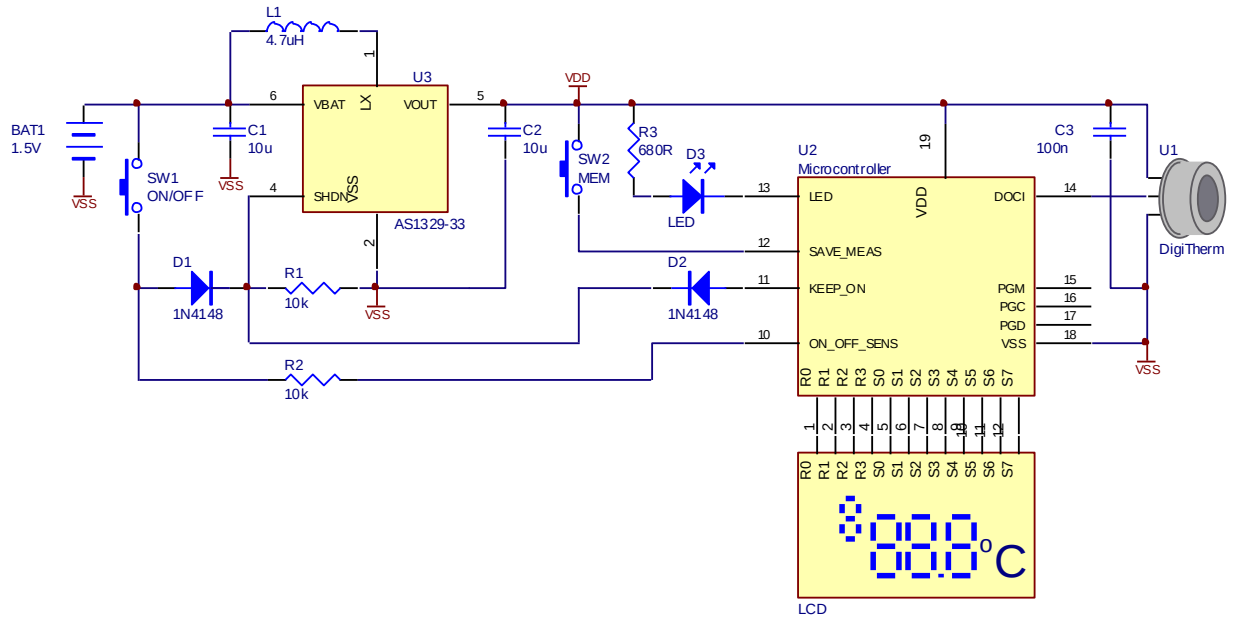
- Compact ear thermometer
- High precision remote temperature sensing
- Infrared pyrometers

Features

- Direct connection to thermopile elements
- Temperature measurement
- Differential analog input
- Digital Signal Processing (DSP)
- Single wire serial interface (DOCI™)
- Operating voltage down to 2.7V
- Low current consumption
- High dynamic range
- High supply rejection

Application Diagram

Compact ear thermometer



Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remarks
Supply Voltage	V_{DD}	-0.3	3.6	V	
Current into any pin		-100	100	mA	One pin at a time
Storage Temperature	T_{ST}	-45	125	°C	

Stresses beyond those listed above may cause permanent damage to the device. Exposure to absolute maximum ratings may affect the device reliability.
ESD protection: all pins will be able to withstand a discharge of a 100pF capacitor charged to 1.6kV through a 1500Ω series resistor. Test method: MIL-STD-883D method 3015.

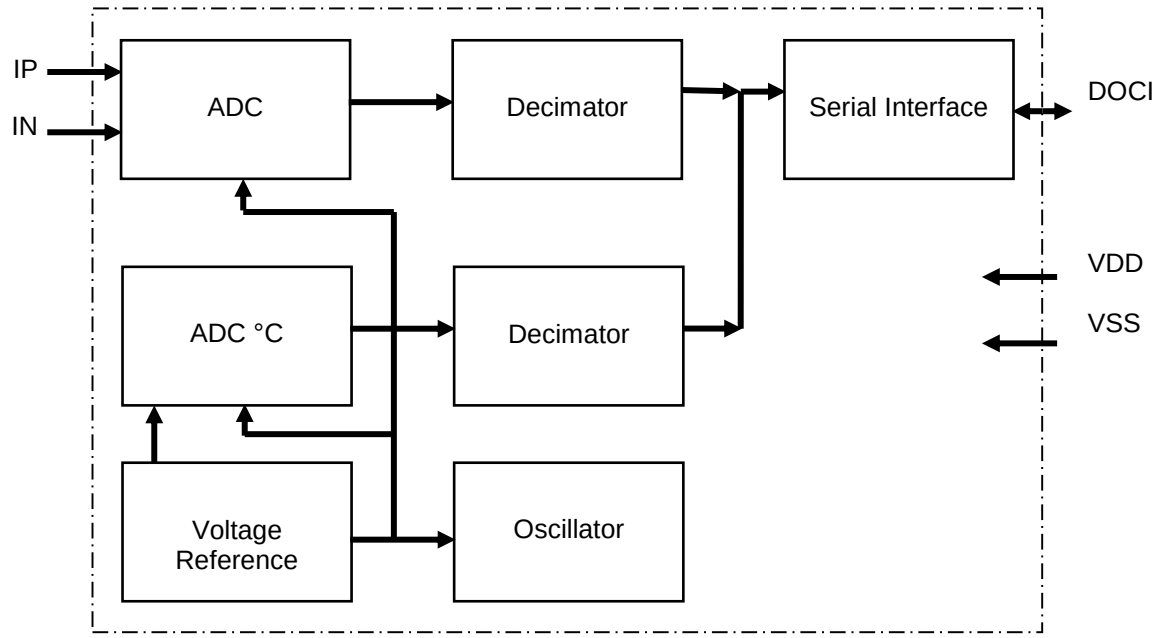
Operating Conditions (T=25°C, unless stated otherwise)

Operating temperature range: -25 to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Supply						
Supply voltage	V_{DD}	2.7	3.3	3.6	V	
Supply current	I_{DD}			15	µA	V_{DD}=3.3V
Digital DOCI interface						
Input low voltage	V_{IL}			20	$\%V_{DD}$	
Input high voltage	V_{IH}	80			$\%V_{DD}$	
Pull down current			200		µA	IN/Out to V_{DD}
Pull up current			130		µA	IN/Out to V_{SS}
Input capacitance			5		pF	
DOCI interface setup time	t_s	2			$1/F_{CLK}$	µC defines T_{REP}
Data clock low time	t_L	200			ns	
Data clock high time	t_H	200			ns	
Data bit settling time	t_{bit}	1			µs	C_{LOAD} = 10pF
DOCI low time to avoid update	$t_L + t_{bit}$			$1/F_{CLK}$		
Serial Interface update time	T_{REP}		32		$1/F_{CLK}$	
Serial Interface update time	T_{REP}		512		$1/F_{CLK}$	E931.08 defines T_{REP}
Analog Inputs (IP/IN), Analog to Digital Converter						
Input Impedance		30	60		MΩ	V_{IN} = -50mV .. +50mV
Input voltage range		-50		50	mV	Differential
		-100		100	mV	Common Mode
ADC Resolution			17		Bits	
ADC Sensitivity		0.7	0.8	0.9	µV/count	
ADC Temperature Coefficient		-300		300	ppm/K	
RMS output noise referred to input						
			0.5		µV/√Hz	@ 1Hz
ADC Offset			64500		counts	
Digital Filter Type & Cut off Freq.	F_0	F_{CLK} * 1.41 / 2048 / PI			Hz	2nd Order BW LPF
Digital Filter Sampling Freq.	F_{ADC}		1/32		F_{CLK}	

Temperature Measurement						
Gain			90		Counts/K	-20ºC to +90ºC
Measurement Range		-20		+90	ºC	
Linearity		-5		5	%	-20ºC to +90ºC
Count Value @ 25 ºC			7900			
Oscillator						
Internal Oscillator Frequency	F_{OSC}		70		kHz	
Internal clock frequency	F_{CLK}		$F_{OSC}/2$			
Temperature Dependency		-1000		1000	ppm/k	-20ºC to +80ºC

Detailed Description



Oscillator
The IC contains an on chip low power oscillator, with a frequency of 70 kHz. All time related signals and the cutoff frequencies of the digital filters are related to the oscillator's frequency.

Analog Inputs and A/D Conversion
The analog to digital converter generates a digital signal from the voltage level measured between the IP and IN terminals.

Decimation
The output signal from the ADC is converted to a 17 bit value by down sampling to Fclk/32.

Temperature Measurement
The on chip temperature is measured by converting the temperature dependent voltage of the reference to a digital value with a resolution of 0.01K.

Parallel to Serial Data Latch

Data is transferred from the decimators to the serial interface whenever new data is available and the DOCI output is not active (being read) or at “H” level. If the micro controller reads the register faster than the update rate of the filter, the data read is “0”.

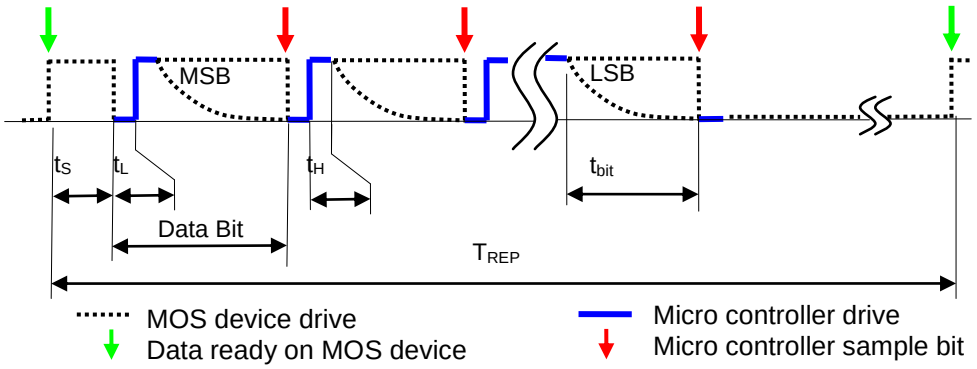
The start of a read cycle is indicated by the M931.08B by pulling DOCI high.
The microcontroller generates a low to high transition on the DOCI line, before is samples the data bit. The first bit read is the MSB. This process is repeated until all 31 bits have been read. After the last bit is read, the microcontroller must force low level and subsequently release DOCI.
When a new ADC value is generated, the M931.08B will pull the DOCI line high and a new data byte can be read. If reading is interrupted for more than 1 system clock with the DOCI interface at low level, the output data latch is updated with new values. Reading can be interrupted, while the DOCI interface is forced high. The output latch is not updated in this condition.

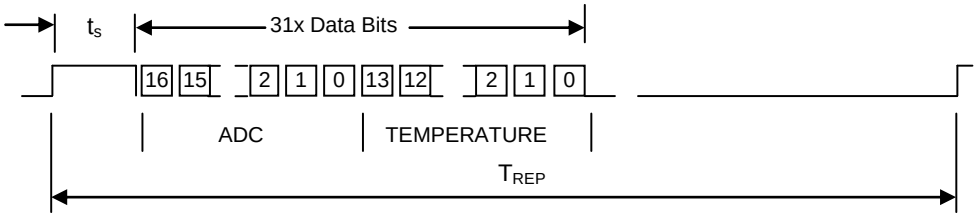
As there is a new filter value available every 32 system clock cycles, the device accepts shorter readout cycles (T_{REP}). To make use of this feature, the microcontroller must force an “H” level on the DOCI line for at least 2 clock cycles (t_S). Thereafter, it can read out the data bits as usual.

The DOCI line must be at “L” level for at least 2 system clock cycles to ensure, that the interface is loaded with new data.

A synchronized or uniform reading is recommended to achieve optimum signal to noise ratio.

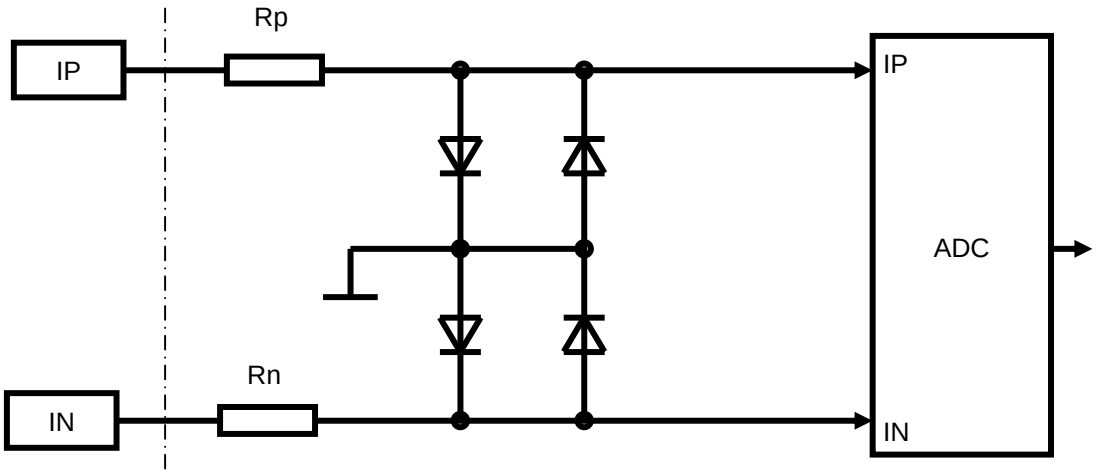
DOCI Interface





T_{REP} = 512 system clocks

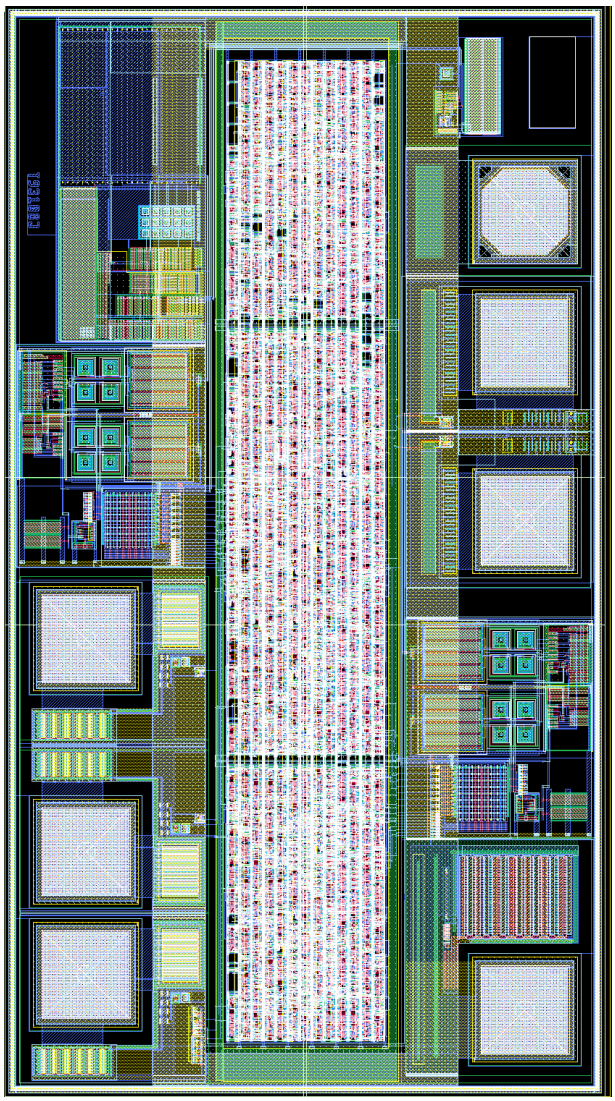
ADC Input Stage



The input impedance of the actual ADC (IP / IN)
is approximately 30MΩ.

Pad Positions

Dimensions without scribe: 660µm x 1190µm
For final step size add scribe width. Example: 100u scribe -> 760µm x 1290µm



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